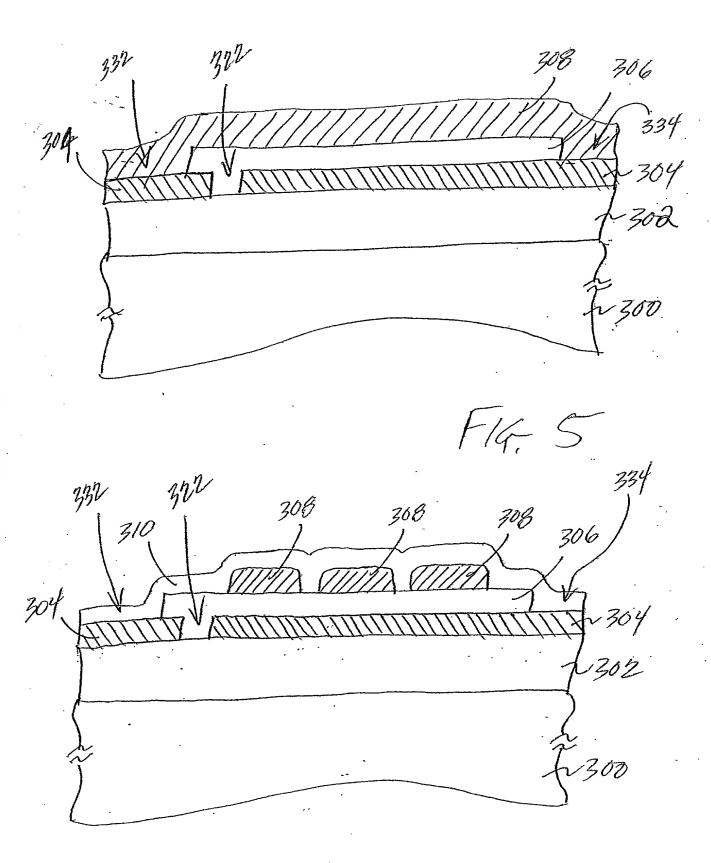


FORM FIRST DIELECTRIC LAYER OVER SEMICONDUCTOR SUBSTRATE W 202	
FORM FIRST MAGNETIC LAYER OVER FIRST DIELECTRIC LAYER WING	
V	
PATTERN FIRST MAGNETIC LAYER TO DEFINE AT LEAST ONE SLOT	
FORM SECOND DIELECTRIC LAYER OVER FIRST MAGNETIC LAYER, FILLING EACH SLOT IN FIRST MAGNETIC LAYER	
PATTERN SECOND DIELECTRIC LAYER TO DEFINE AT LEAST ONE VIA TO FIRST MAGNETIC LAYER	
FORM CONDUCTIVE LAYER OVER SECOND DIELECTRIC LAYER WILL	
· · · · · · · · · · · · · · · · · · ·	
PATTERN CONDUCTIVE LAYER TO FORM A CONDUCTOR HAVING A SPIRAL-SHAPED SIGNAL PATH AND TO CLEAR ANY VIAS TO FIRST MAGNETIC LAYER	
FORM THIRD DIELECTRIC LAYER OVER CONDUCTIVE LAYER JULY	
PATTERN THIRD DIELECTRIC LAYER TO DEFINE AT LEAST ONE VIA TO FIRST MAGNETIC LAYER	
· · · · · · · · · · · · · · · · · · ·	
FORM SECOND MAGNETIC LAYER OVER THIRD DIELECTRIC LAYER, FILLING ANY VIAS TO FIRST MAGNETIC LAYER	
PATTERN SECOND MAGNETIC LAYER TO FORM AT LEAST ONE SLOT	

F14.3

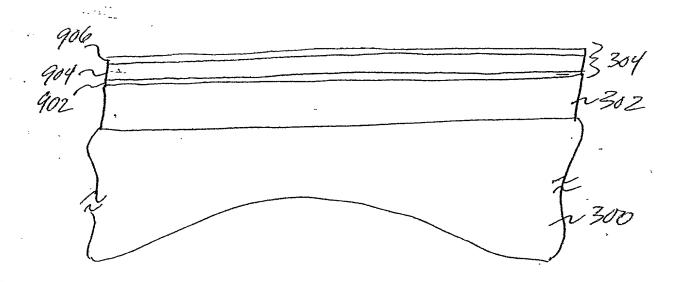


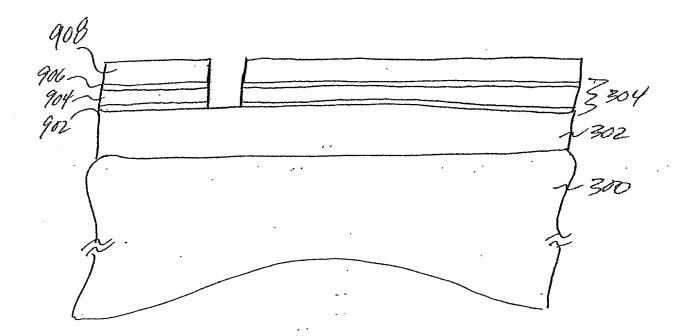
33h 3h 3h 308 308 308 306 306 334 309 1302 300

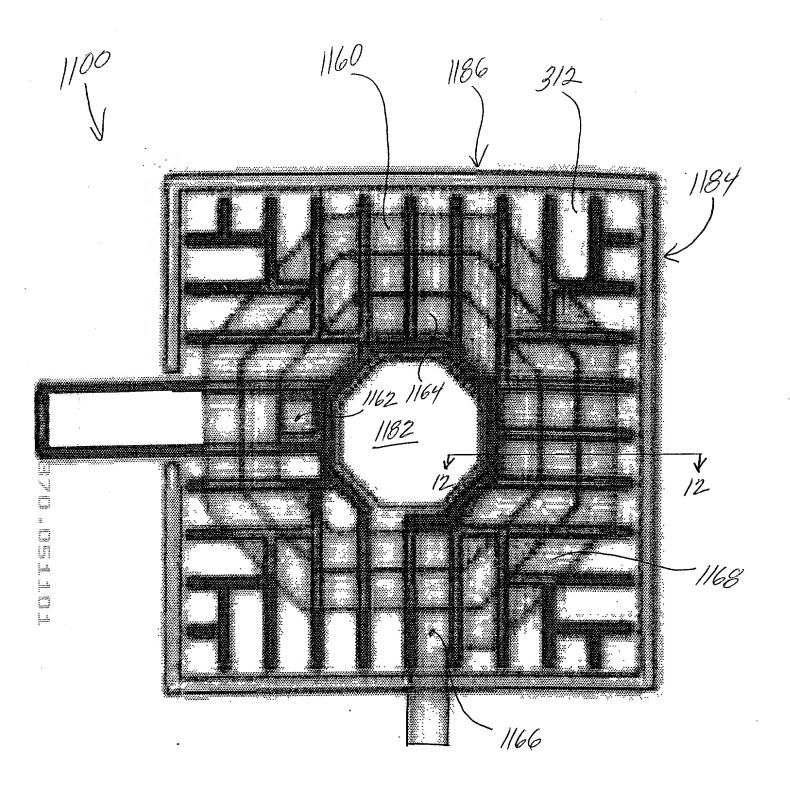
90	\mathcal{O}
	9

FORM UNDERLYING LAYER OVER DIELECTRIC LAYER BOZ FORM MAGNETIC MATERIAL LAYER OVER UNDERLYING LAYER BOY FORM OVERLYING LAYER OVER MAGNETIC MATERIAL LAYER BOS FORM PATTERNED MASK LAYER OVER OVERLYING LAYER BOS

ETCH UNDERLYING, MAGNETIC MATERIAL, AND OVERLYING LAYERS

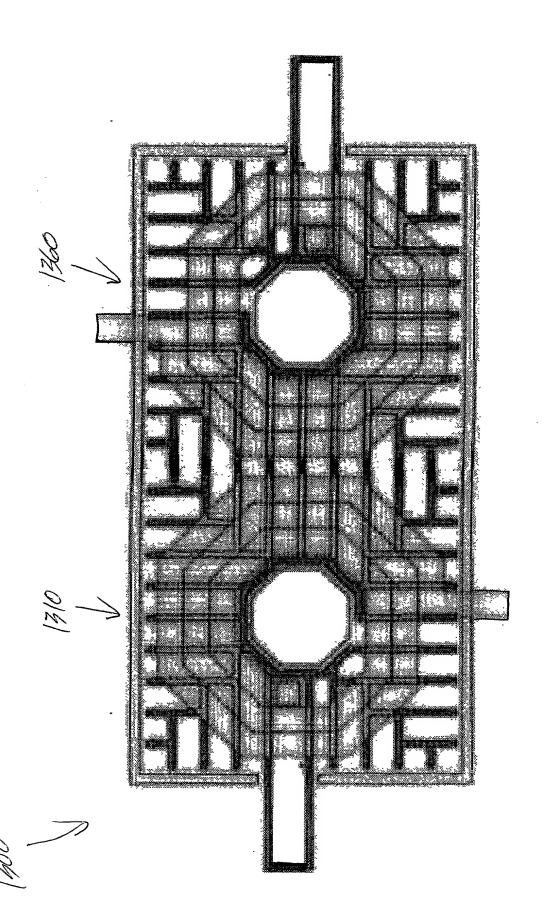




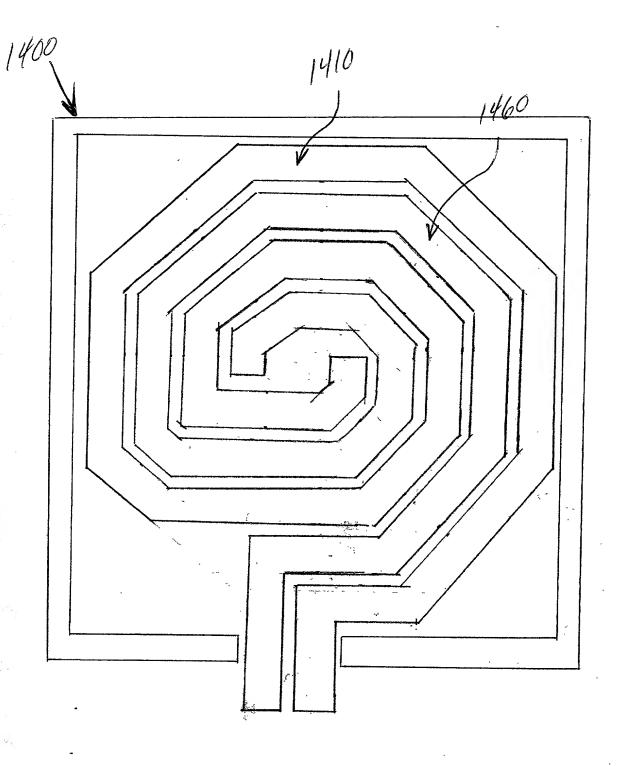


1/50
316
316
316
316
318
318
319
310
310
310
310
310
306
310
307
307
307
307
307

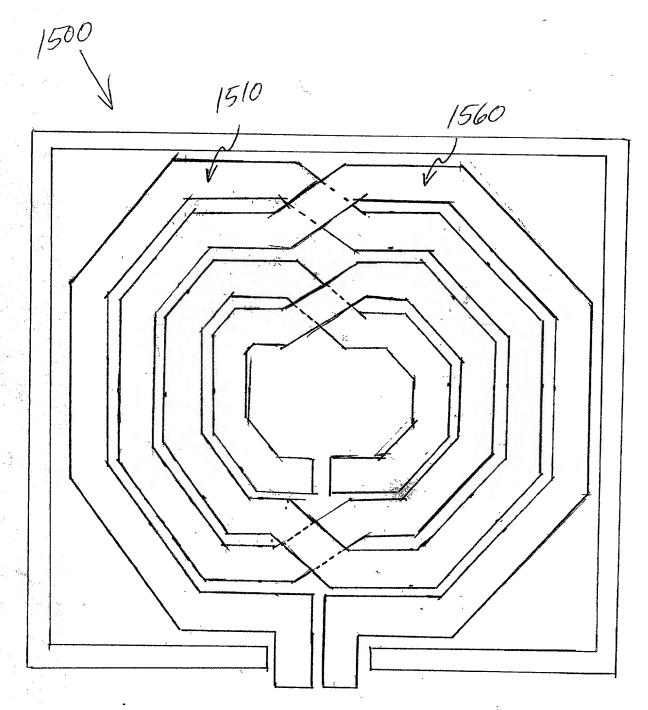
1100

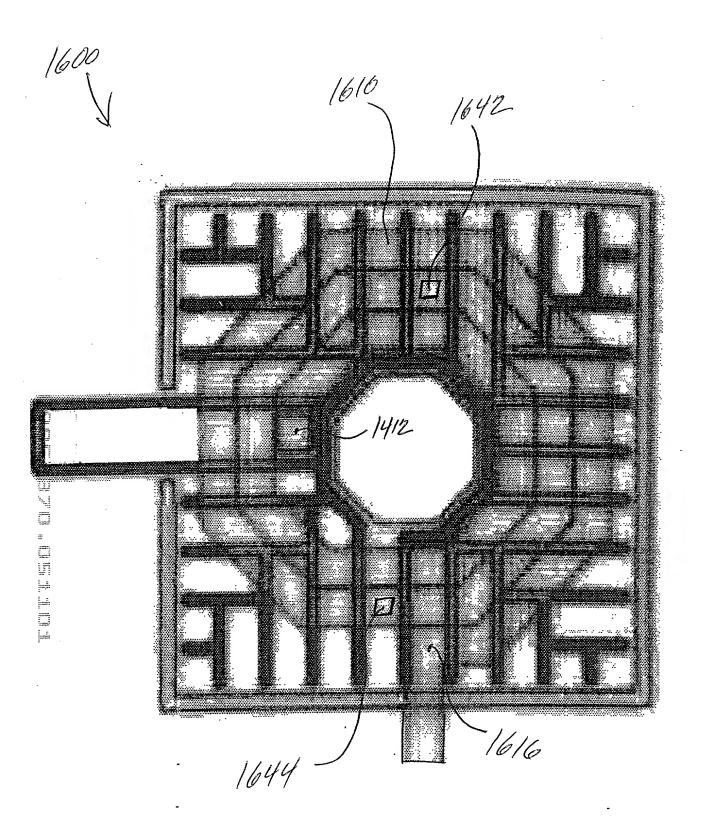


F14 13



F14.14





1800

TRANSFORMER	DEVICE 1/704 1/700
TRANSFORMER 1702	DEVICE MARK
INTEGRATED CIRCU	UT
	F14, 17

INTEGRATED N 1804
CIRCUIT

(1802
(1802
TRANSFORMER
TRANSFORMER

INTEGRATED CIRCUIT PACKAGE